WHAT IS CLAIMED IS:

1. A synchronous bank memory comprising:

a plurality of first layer modules, each of which including a bank consisting of a plurality of 1-port memory cells and a port transition circuit between 1 port and N ports;

a clock generator which generates an internal clock signal and sends the internal clock signal to said plurality of first layer modules;

registers and buffers which receive a read/write signal and an address signal from each of external ports, receive and send a data signal to and from each of the external ports, and receive and send a port block signal;

an access conflict management circuit which receives the address signals from said registers and buffers and generates the port block signal when an access conflict to a bank occurs;

a bank column selector arranged between said registers and buffers and said plurality of banks, which receives the read/write signal and the address signal from said registers and buffers and the data signal from said registers and buffers or said plurality of banks, generates a bank column selection signal based on the address signal to output it to said plurality of banks; and

a bank row selector which receives the address signal

from said registers and buffers and generates a bank row selection signal based on the address signal to output it to said plurality of banks selected by the bank row selection signal among said plurality of banks;

wherein said port transition circuit activates a bank among said plurality of banks based on the bank column selection signal and bank row selection signal when no port block signal is outputted by said access conflict management circuit.

2. The synchronous bank memory according to claim 1, including static CMOS gates;

wherein said port transition circuit comprises an active-address-connect circuit which selects an address, an active-data-connect circuit which selects a data, and a bank-enable controller which controls said active-address-connect circuit and said active-data-connect circuit;

said bank-enable controller generates an address switch enable signal and a precharge control signal for address lines in said active-address-connect circuit, based on the read/write signal, the row and column selection signals and the port block signals for each port, and sends the generated signals to said active-address-connect circuit;

said bank-enable controller generates a read access enable signal and a write access enable signal for each

port and a precharge control signal for data lines in said active-data-connect circuit and sends them to said active-data-connect circuit; and

said bank-enable controller generates a control clock signal in the bank based on the internal clock signal from said clock generator.

3. The synchronous bank memory according to claim 1, including dynamic CMOS gates and dynamic CMOS latch circuits, wherein said access conflict management circuit and said port transition circuit receive the internal clock signal to control said dynamic CMOS gates in said access conflict management circuit and said port transition circuit and to control said dynamic CMOS latch circuits for latching data when the dynamic CMOS gates enter a precharge period.

4. The synchronous bank memory according to claim 3, wherein said port transition circuit comprises an active-address-connect circuit which selects an address, an active-data-connect circuit which selects a data, and a bank-enable controller which controls said active-address-connect circuit and said active-data-connect circuit;

said bank-enable controller generates an address switch enable signal and a precharge control signal for address lines in said active-address-connect circuit, based on the read/write signal, the row and column selection

signals and the port block signals, and sends them to said active-address-connect circuit;

said bank-enable controller generates a read access enable signal and a write access enable signal for each port and a precharge control signal for data lines in said active-data-connect circuit and sends them to said active-data-connect circuit; and

said bank-enable controller generates a control clock signal in the bank based on the internal clock signal from said clock generator.

5. The synchronous bank memory according to claim 4, wherein said active-address-connect circuit comprises an NMOS transmission gate as a gate for sending the address signal to the bank.

6. The synchronous bank memory according to claim 4, wherein said active-data-connect circuit comprises an NMOS transmission gate as a gate for sending the data signal to the bank.

7. The synchronous bank memory according to claim 3, wherein said access conflict management circuit comprises a multi-input EXNOR gate made of dynamic CMOS gates, the multi-input EXNOR gate receives an address signal and its inverted signal form the ports to generates a signal which represents whether access conflict occurs between addresses of a pair of ports in the ports.

8. The synchronous bank memory according to claim 3, wherein said access conflict management circuit comprises OR gates of signals which represent whether an access conflict happens on addresses of a pair of ports in the ports and a port disable signal, an AND gate of results of all the OR gates, and an output circuit which sends an output of the AND circuit as the port block signal.

9. The synchronous bank memory according to claim 3, wherein said access conflict management circuit comprises a circuit for giving priority to a port of a smaller port number, another circuit for giving priority to a port of a larger port number, and a selector which selects one of outputs of the two circuits to output the port block signal.

10. A synchronous bank memory comprising:

a plurality of banks including of a plurality of 1-port memory cells;

a clock generator which generates an internal clock signal and sends the internal clock signal to said plurality of banks;

registers and buffers which receive a read/write signal and an address signal from each of external ports, receive and send a data signal to and from each of the external ports, and receive and send a port block signal;

an access conflict management circuit which receives the address signals from said registers and buffers and

generates the port block signal when an access conflict occurs; and

a crossbar switching network, provided between said registers and buffers and said plurality of banks, performing switching at cross points at a plurality of nodes, each of the nodes being located between a line connected to the ports and signal lines from said banks, wherein said crossbar switching network receives the read/write signal and the address signal from said registers and buffers and the data signal from said registers and buffers or said plurality of banks, activates one of the cross points based on the address signal when no port block signal is outputted by said access conflict management circuit.

11. A synchronous bank memory comprising:

a plurality of banks including of a plurality of 1-port memory cells;

a clock generator which generates an internal clock signal and sends the internal clock signal to said plurality of banks;

registers and buffers which receive a read/write signal and an address signal from each of external ports, receive and send a data signal to and from each of the external ports, and receive and send a port block signal;

an access conflict management circuit which receives

the address signals from said registers and buffers and generates the port block signal when an access conflict occurs; and

a plurality of crossbar switching networks provided between said registers and buffers and a plurality of clusters into which said plurality of banks are divided, wherein each of said plurality of crossbar switching networks performs switching at cross points at nodes, each of the nodes being located between lines connected to the ports and a signal line from each bank in a cluster;

wherein each of said crossbar switching networks receives the read/write signal and the address signal from said registers and buffers and the data signal from said registers and buffers or said plurality of banks, activates a cross point based on the address signal when no port block signal is outputted by said access conflict management circuit.

12. A synchronous bank memory comprising:

a plurality of banks including a plurality of 1-port memory cells;

a clock generator which generates an internal clock signal and sends the internal clock signal to said plurality of banks;

registers and buffers which receive a read/write signal and an address signal from each of external ports,

receive and send a data signal to and from each of the external ports, and receive and send a port block signal;

an access conflict management circuit which receives the address signals from said registers and buffers and generates the port block signal when an access conflict occurs; and

a network provided between said registers and buffers and said plurality of banks, wherein said network receives the read/write signal and the address signal from said registers and buffers and the data signal from said registers and buffers or said plurality of banks, generates a bank selection signal when no port block signal is outputted by said access conflict management circuit, and activates the bank selected by the bank selection signal.

13. A synchronous bank memory comprising:

a plurality of banks including a plurality of 1-port memory cells;

a clock generator which generates an internal clock signal and sends the internal clock signal to said plurality of banks;

registers and buffers which receive a read/write signal and an address signal from external ports, receive and send a data signal to and from external ports, and receive and send a port block signal; and

a network, provided between said registers and buffers

and said plurality of banks, wherein said network receives the read/write signal and the address signal from said registers and buffers, generates a bank selection signal to activate the bank selected by the bank selection signal.

14. A method for accessing a synchronous bank memory including a plurality of banks each including a plurality of 1-port memory cells, a clock generator which generates an internal clock signal, registers and buffers which receive a read/write signal and an address signal from each of external ports, receive and send a data signal to and from each of the external ports, and a switching network provided between said registers and buffers and said plurality of banks;

wherein when a clock cycle is started, the registers and buffers send the read/write signal and the address signal to the switching network and send the address signals to the access conflict management circuit, the switching network generates a bank selection signal when a port block signal is not received from the access conflict management circuit, and a bank in the plurality of banks, all of which are in precharged state for read/write state for read/write operation, is selected by the bank selection signal; and

when the selected bank receives an internal clock signal from the clock generator, memory cells in the bank

are accessed, and if read is instructed, the read data is sent to the port.

15. A method for accessing a synchronous bank memory including a plurality of banks each including a plurality of 1-port memory cells, a clock generator which generates an internal clock signal, registers and buffers which receive a read/write signal and an address signal from an external port, receive and send a data signal to and from the external ports, and a switching network provided between the registers and buffers and the plurality of banks;

wherein when a clock cycle is started, the registers and buffers send the read/write signal and the address signal to the switching network, the switching network generates a bank selection signal, and when the bank selection signal is received, a bank, being in precharged state for read/write operation, is selected by the bank selection signal; and

when the selected bank receives an internal clock signal from the clock generator, a memory cell in the bank is accessed, and if read is instructed, the data is sent to the port.